1b.3

D-band SiGe Subharmonic Downconverter with Dynamic Conversion Gain and Fixed Input Compression

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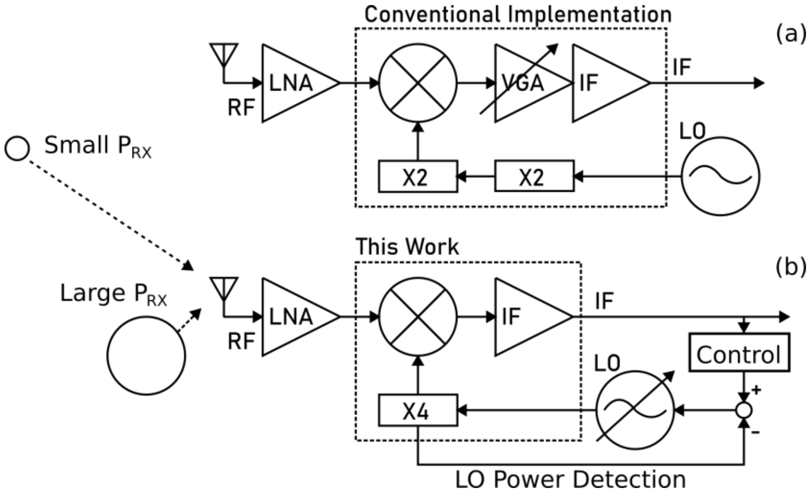
Motivation

- Power consumption above 100 GHz is prohibitive:
  - mobile applications
  - Radar-radio fusion on platform

- LO system power dominates receiver power consumption

- **Reduce power in LO chain dynamically with channel conditions**



Goals of This Work

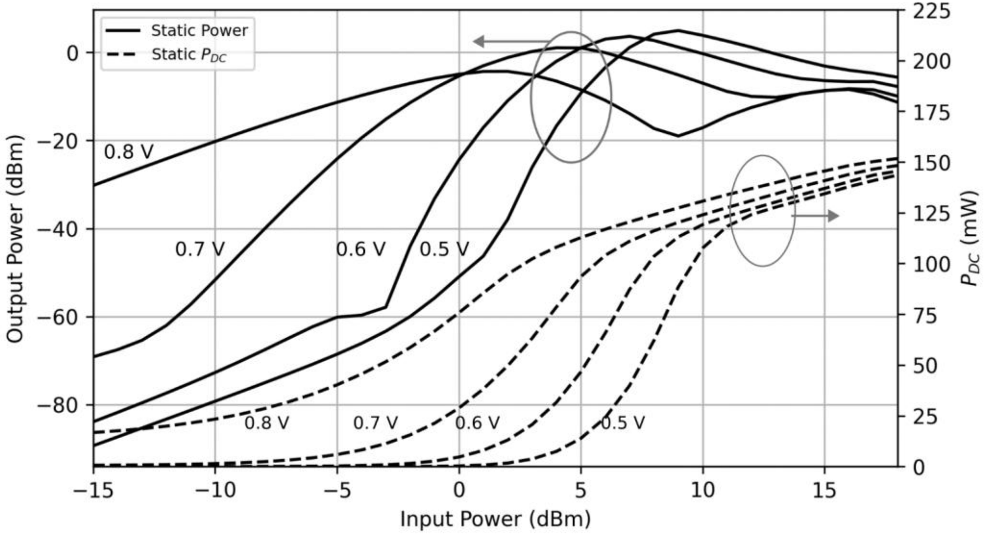
X4 Subharmonic downconverter at D-band (110 GHz – 170 GHz)

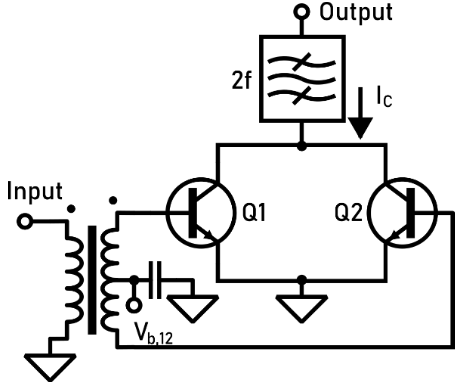
1. Linearize gain on LO frequency multiplier
   - backoff controllability to save power

2. Simplify circuit to save power and to integrate into an array

Problem: Gain Sensitivity

- Typical multiplier chains operate at a single saturating power
- High gain sensitivity in back-off power conditions: poor controllability





Simulation on frequency doubler with different biases for optimization

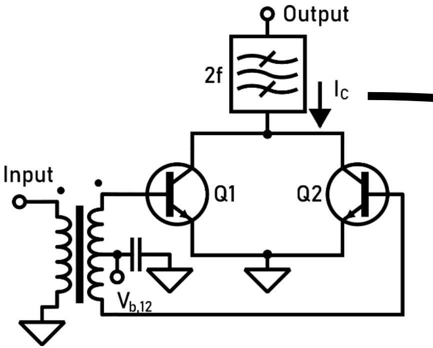
Push-pull Frequency Multipliers

- Input is rectified to produce pulsed waveform
- We can get a 4th harmonic
- **But there is an additional DC current**
  - Affects biasing and gain
  - Causes extreme gain sensitivity to power

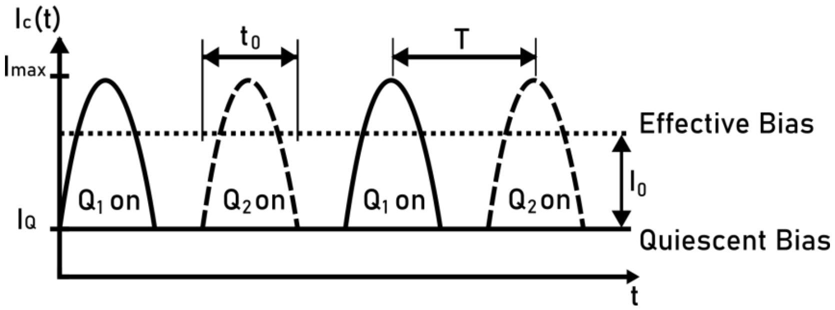
$$I_c(t) = I_0 + I_1 cos(\omega t) + I_2 cos(2\omega t) + \ \dots\ I_n cos(n\omega t)$$

Fourier Series

$$I_n = I_{max}\frac{4t_0}{\pi T}\begin{cases}1 & \text{, if } n=0\\ 2\cdot\left|\frac{\cos\left(\frac{n\pi t_0}{T}\right)}{1-\left(\frac{n\pi t_0}{T}\right)^2}\right| & \text{, if } n \text{ even}\\ 0 & \text{, if } n \text{ odd}\end{cases}$$



Conventional Multiplier

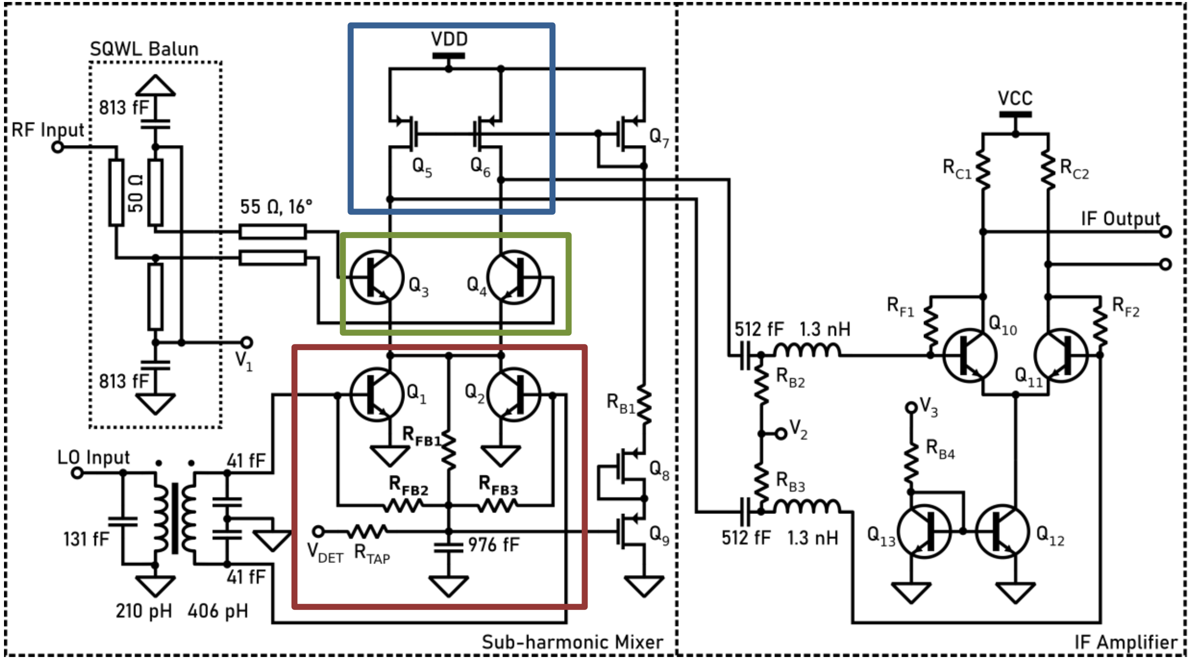


Proposed Downconverter

Active Load

Mixer

X4 Frequency Multiplier



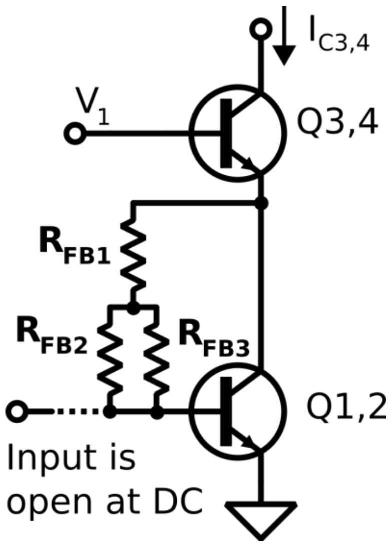
VDD VCC	3 V
V_1	1.5 V
V_1 V_3 V_2	1 V

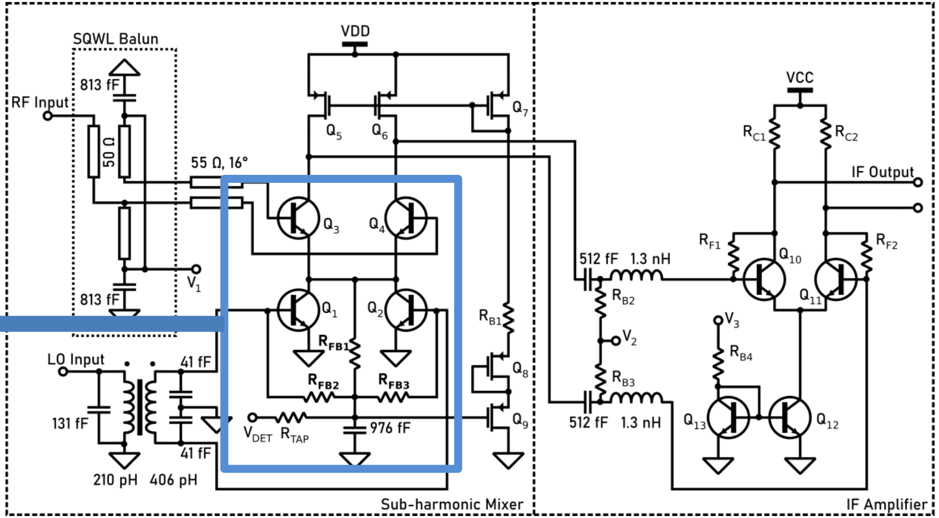
Q_1 Q_2	6 um
Q_3 Q_4	10 um
Q_5 Q_6	0.1 x 40 um
Q_7	0.1 x 2 um
Q_8 Q_9	0.1 x 10 um
Q_{10} Q_{11}	4 um
Q_{12}	6 um
Q_{13}	0.5 um

R_{FB1}	1 kΩ
$R_{FB2}R_{FB3}$	3.5 kΩ
R_{C1} R_{C2}	200 Ω
R_{F1} R_{F2}	800 Ω
R_{B1}	1 kΩ
R_{B2} R_{B3}	5 kΩ
R_{B4}	300 kΩ
R_{TAP}	500 Ω

Feedback Bias Analysis

Equivalent DC Model





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Proposed Design: Feedback Bias

- Parallel transistors shorted at DC: treat as one
- Simplifying assumptions:

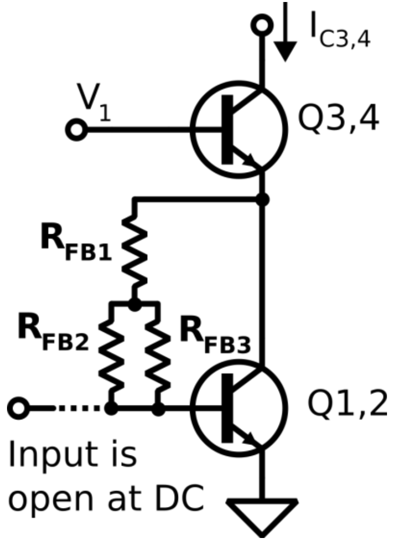
$$V_{BE1,2} \approx V_{BE3,4} \qquad I_{C3,4} \approx I_{C1,2}$$

- **Feedback Bias has stable bias point:**

$$I_{C3,4} = \beta_{1,2} \frac{V_1 - 2V_{BE}}{R_{FB1} + R_{FB2} || R_{FB3}}$$

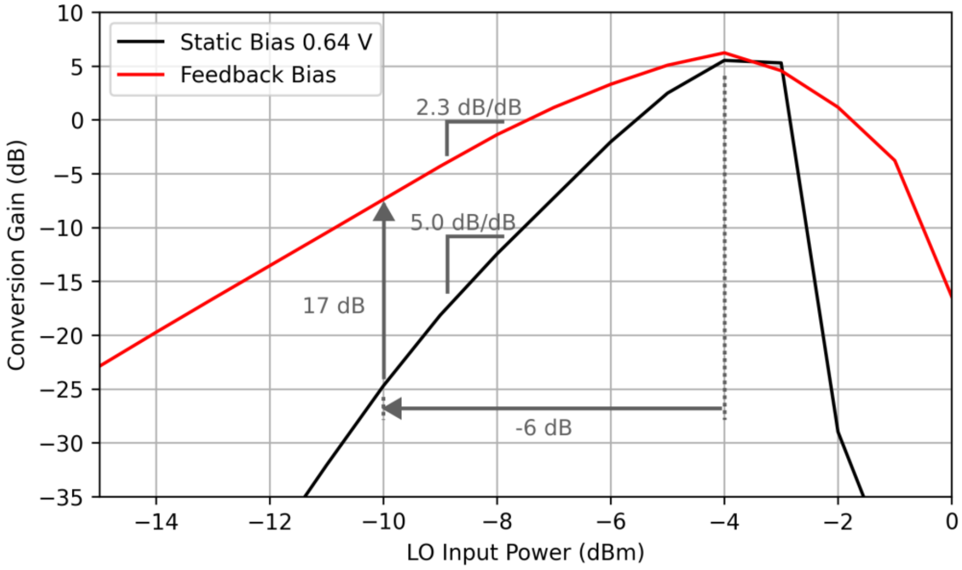
- **Current change suppressed by negative feedback on V_{BE}**

Equivalent DC Model



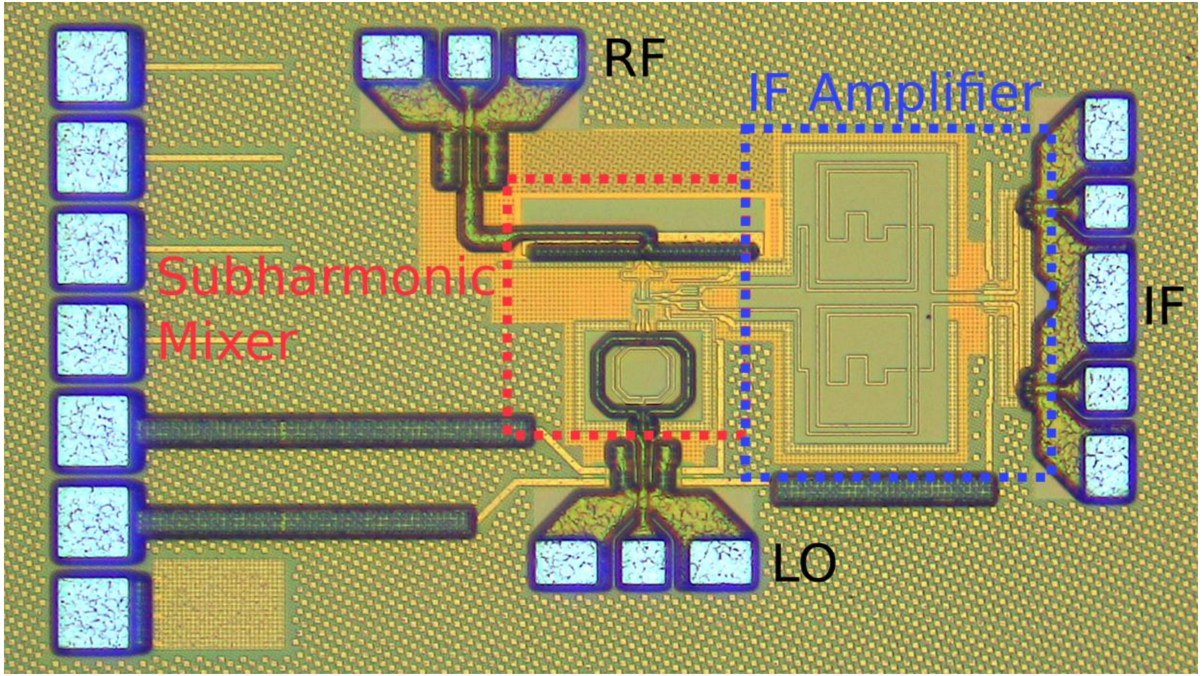
Simulated Effect of Static Biasing

- With -6 dB LO backoff from peak gain
  - 17 dB more gain than static biased version
- Obtain higher performance at back-off and less sensitive gain



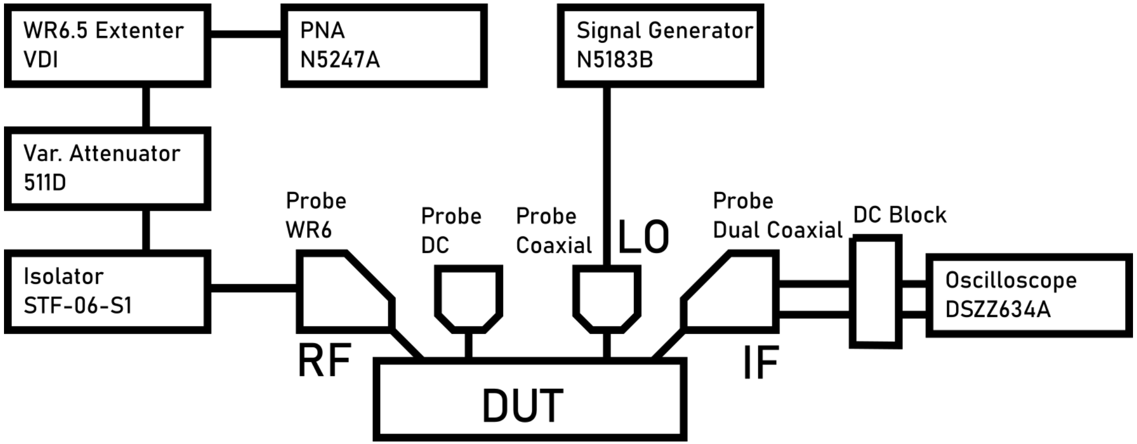
Layout

- Global Foundries 9HP+
  - 90-nm SiGe BiCMOS
- Core: 0.56 mm x 0.35 mm



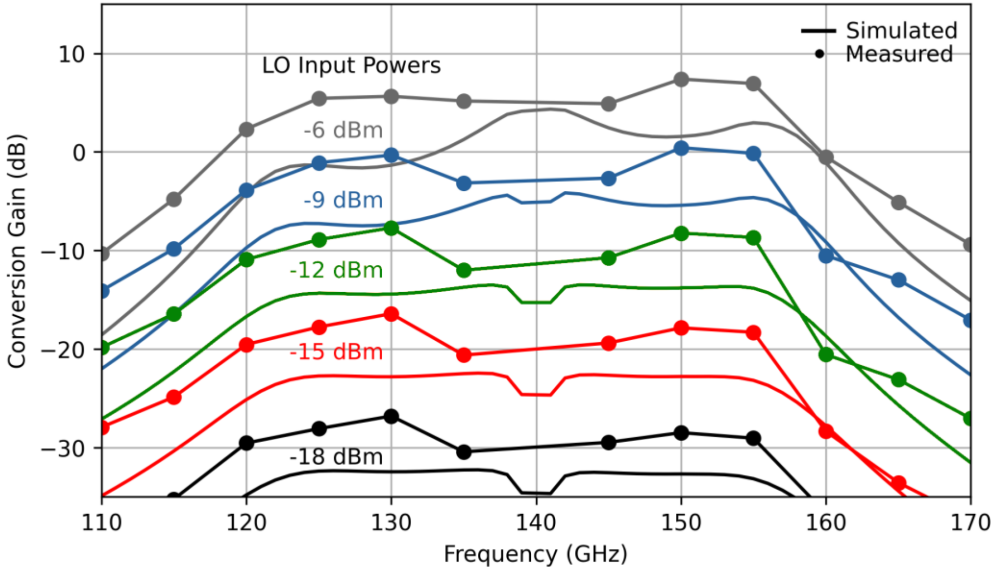
Measurement

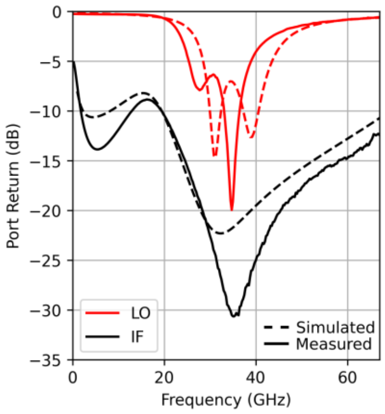
- Results calibrated with reference power meter (scalar measurement)
- Differential mismatch compensated with time delay in oscilloscope

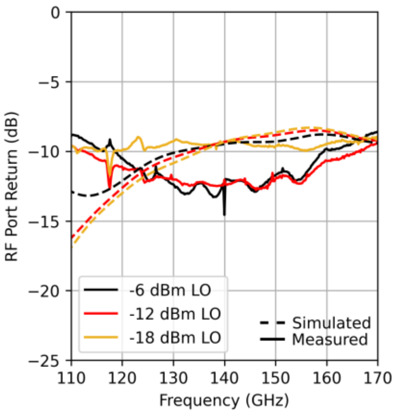


Conversion Gain Over Frequency

- Reliable control of conversion gain over a wide LO power range
- LO port frequency shift led to better match at target LO frequency

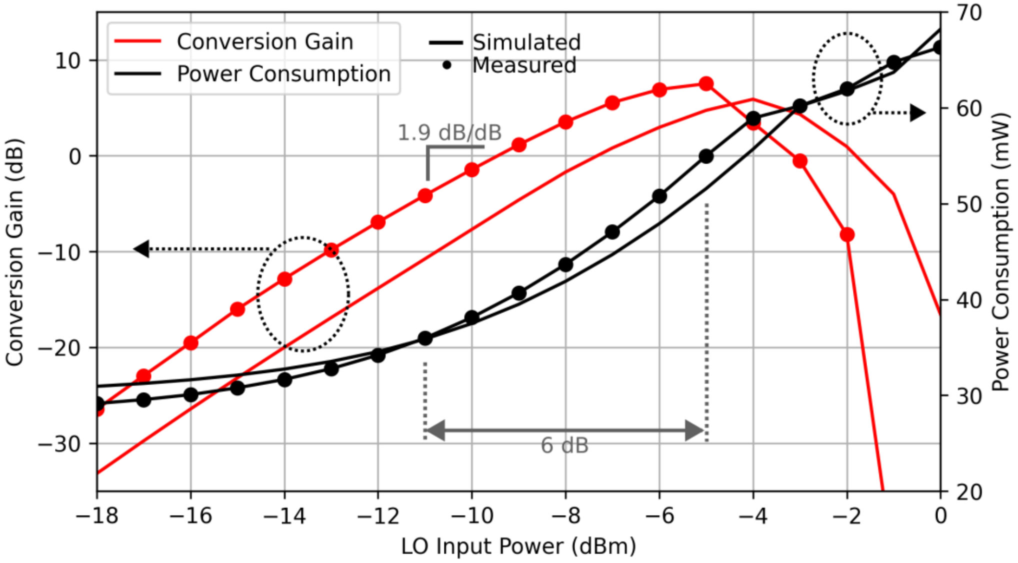






Power Consumption Tradeoff

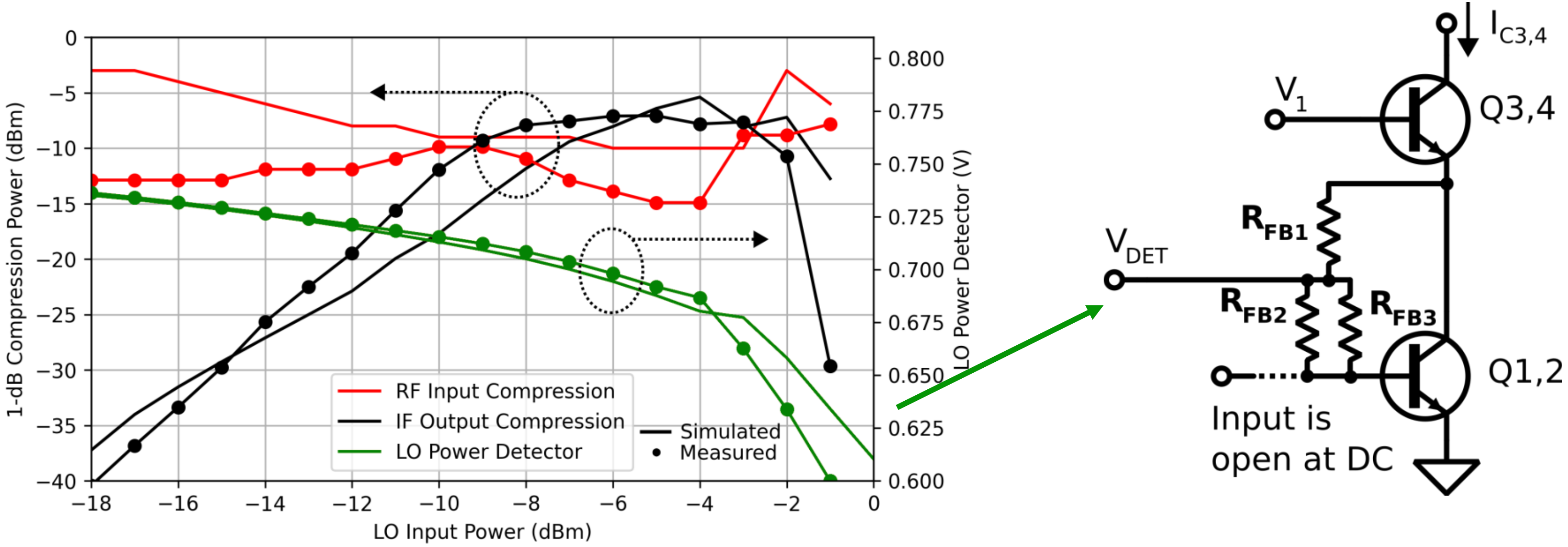
- Back off LO power from -5 dBm to -11 dBm
  - **Trade 11.7 dB of gain to save 35% power**



155 GHz RF with 140 GHz LO

Compression and Power Detector

- Input compression is insensitive to LO power variation
- Feedback bias circuit can be used for LO power detection



Conclusion

- A fourth subharmonic D-band downconverter is implemented with bias feedback
  - Demonstrates reliable LO power backoff to save power
- Achieves a high multiplication factor without sacrificing additional area, power consumption, or LO power requirement

Reference	This Work	[3]	[6]	[7]
Technology	90-nm SiGe	90-nm SiGe	130-nm SiGe	130-nm SiGe
Subharmonic	4	2	2	1
f_C (GHz)	140	136	121	140
BW_{3dB} (GHz)	35	38	>14	35
Gain (dB)	7.5	5.1	4	32
P_{i1dB} (dBm)	-15	-7	-	-41
Noise Figure (dB)	21.7*	-	23*	9.5
LO (dBm)	-5	2	7	-2
P_{DC} (mW)	55	51	89	65
Area (mm^2)	0.196†	0.450†	-	0.191†

* Simulated † Area without pads.

Acknowledgements

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Comparison References

[3] A. Moradinia, Y. A. Mensah, B. L. Ringel, and J. D. Cressler, "A 117–155-GHz SiGe HBT D-Band Subharmonic Mixer Utilizing a Novel 180° Hybrid Coupler," IEEE Microwave and Wireless Technology Letters, vol. 33, no. 6, pp. 731–734

[6] K. Schmalz, W. Winkler, J. Borngr¨aber, W. Debski, B. Heinemann, and J. C. Scheytt, "A Subharmonic Receiver in SiGe Technology for 122 GHz Sensor Applications," IEEE Journal of Solid-State Circuits, vol. 45, no. 9, pp. 1644–1656,

[7] T. Maiwald, J. Potschka, K. Kolb, M. Dietz, A. Hagelauer, A. Visweswaran, and R.Weigel, "A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 7, pp. 2277–2281